CXP 120G 300M MMF SR10

SLCX-120G-SR10

Overview

Sourcelight 120G CXP transceiver modules is a high performance, low power consumption, long reach interconnect solution supporting 120G Ethernet, Infiniband QDR DDR SDR 1G/2G/4G/8G/10G fiber channel and PCIE. It is compliant with the 120Gbits Small Form factor Hot-Pluggable CXP-interface.

Sourcelight 120G CXP transceiver modules is an assembly of 12 full-duplex lanes, where each lane is capable of transmitting data at rates up to 10.5Gb/s, providing an aggregated rate of 120Gb/s.

Features

- 12-channel full-duplex transceiver module
- Hot Pluggable CXP footprint
- Maximum link length of 300m on OM3 or 400m on OM4 Multimode Fiber (MMF)
- Multirate capability: 1.06Gb/s to 10.5Gb/s per CH
- Unretimed CPPI electrical interface
- Requires 3.3V power supply only
- Low power dissipation: <4.5W
- Reliable VCSEL array technology
- Built-in digital diagnostic functions
- Commercial operating case temperature : 0℃ to 70℃
- Single MPO connector receptacle
- RoHS-6 Compliant (lead-free)

Applications

- 100GBASE-SR10 100G Ethernet
- Multiple 1G/2G/4G/8G/10G Fibre Channel
- Infiniband transmission at 12ch SDR, DDR and QDR
- Switches, Routers
- Data Centers
- Other 120G Interconnect Requirement

Ordering Information

Part Number	Product Description
SLCX-120G-SR10	CXP Optical Transceivers 12Channel X 10.5Gb/s MPO24 OM3 300m 0~70℃

Module Block Diagram

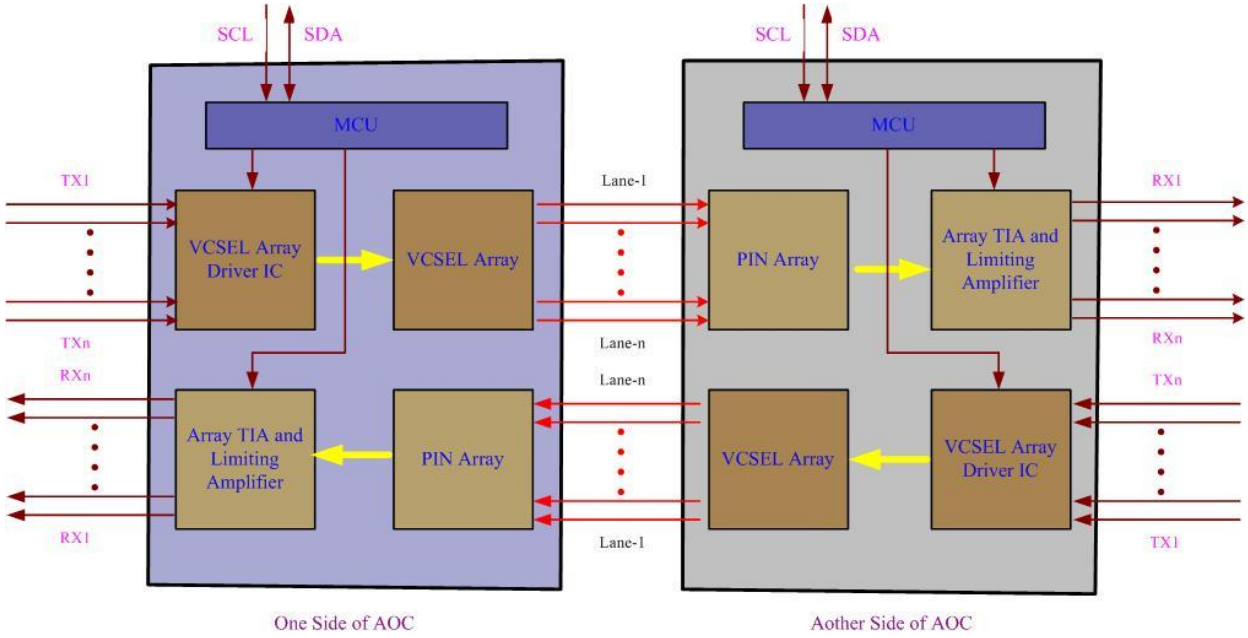

Figure1. Module Block Diagram

General Product Characteristics

Parameter	Value	Unit	Note
Module Form Factor	CXP		
Number of Lanes	12 Tx and 12 Rx		
Maximum Aggregate Data Rate	126	Gb/s	
Maximum Data Rate per Lane	10.5	Gb/s	
Protocols Supported	Typical applications include 100G Ethernet, Infiniband, Fibre Channel, SATA/SAS3		
Electrical Interface and Pin-out	84-pin edge connector		Pin-out as defined by the CXP Specification
Optical Cable Type Required	Multimode ribbon 24-fiber cable assembly, MPO connector		
Maximum Power Consumption per End	4.5	Watts	Varies with output voltage swing and pre-emphasis settings
Management Interface	Serial, I2C-based, 450 kHz maximum frequency		As defined by the CXP Specification

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	ºC
Case Operating Temperature	Top	0	70	ºC
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	ºC
Data Rate Per Lane	fd	1.06		10.5	Gbps
Humidity	Rh	5		85	%
Power Dissipation	Pm			4.5	W

Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage amplitude aAmplitude	ΔVin	200		1200	mVp-p
Differential output voltage amplitude	ΔVout	600		800	mVp-p
Skew	Sw			300	ps
Bit Error Rate	BR			E-12	
Input Logic Level High	VIH	2.0		VCC	V
Input Logic Level Low	VIL	0		0.8	V
Output Logic Level High	VOH	VCC-0.5		VCC	V
Output Logic Level Low	VOL	0		0.4	V

Note:

1. BER=10^-12; PRBS 2^31-1@10.3125Gbps.
2. Differential input voltage amplitude is measured between TxnP and TxnN
3. Differential output voltage amplitude is measured between RxnP and RxnN.

Electrical Characteristics

NOTE: The requires that a CPPI-compliant CXP electrical connector be used on the host board in order to guarantee its electrical interface specification. Please check with your connector supplier.

Parameter	Symbol	Min	Typical	Max	Unit	Ref.
Supply Voltage	Vcc1, VccTx, VccRx	3.15	3.3	3.45	V	
Supply Current	Icc	950		1050	mA	
Module Total Power	P			3.5	W	1
Link Turn-On Time						
Transmit turn-on time				2000	ms	2
Transmitter (per Lane)						
Single ended input voltage tolerance	VinT	-0.3		4.0	V	
Differential data input swing	Vin,pp	120		1200	mVpp	3
Differential input threshold			50		mV	
AC common mode input voltage tolerance (RMS)		15			mV	
Differential input return loss		Per IEEE 802.3ba, Section 86A.4.1.1			dB	4
J2 Jitter Tolerance	Jt2	0.17			UI	
J9 Jitter Tolerance	Jt9	0.29			UI	
Data Dependent Pulse Width Shrinkage	DDPWS	0.07			UI	
Eye mask coordinates {X1, X2 Y1, Y2}		0.11, 0.31 95, 350			UI mV	5
Receiver (per Lane)						
Single-ended output voltage		-0.3		4.0	V	
Differential data output swing	Vout,pp	0		800	mVpp	6,7
AC common mode output voltage (RMS)				7.5	mV	
Termination mismatch at 1 MHx				5	%	
Differential output return loss		Per IEEE 802.3ba, Section 86A.4.2.1			dB	4
Common mode output return loss		Per IEEE 802.3ba, Section 86A.4.2.2			dB	4
Output transition time, 20% to 80%		28			ps	
J2 Jitter output	Jo2	0.42			UI	
J9 Jitter output	Jo9	0.65			UI	
Eye mask coordinates {X1, X2 Y1, Y2}		0.29, 0.5 150, 425			UI mV	5
Power Supply Ripple Tolerance	PSR	50			mVpp	

Notes:

1. Maximum total power value is specified across the full temperature and voltage range.
2. From power-on and end of any fault conditions.
3. After internal AC coupling. Self-biasing 100 Ohm differential input.
4. 10 MHz to 11.1 GHz range

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Ref.
Transmitter (per Lane)						
Signaling Speed per Lane			10.5		GBd	1
Center wavelength		840		860	nm	
RMS Spectral Width	SW			0.65	nm	
Average Launch Power per Lane	TXPx	-7.6		2.4	dBm	
Transmit OMA per Lane	TxOMA	-5.6		3.0	dBm	2
Difference in Power between any two lanes [OMA]	DPx			4.0	dB	
Peak Power per Lane	PPx			4.0	dBm	
Launch Power [OMA] minus TDP per Lane	P-TDP	-6.5			dBm	
TDP per Lane	TDP			3.5	dBm	
Optical Extinction Ratio	ER	3.0			dB	
Optical Return Loss Tolerance	ORL			12	dB	
Encircled Flux	FLX	> 86% at 19 um < 30% at 4.5 um			dBm	
Average launch power of OFF transmitter, per lane				-30	dBm	
Relative Intensity Noise	RIN			-128	dB/Hz	3
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}		0.23, 0.34, 0.43, 0.27, 0.35, 0.4				
Receiver (per Lane)						
Signaling Speed per Lane			10.5		GBd	4
Center wavelength		840		860	nm	
Damage Threshold	DT	3.4			dBm	
Average Receive Power per Lane	RXPx	-9.5		2.4	dBm	
Receive Power (OMA) per Lane	RxOMA			3.0	dBm	
Stressed Receiver Sensitivity (OMA) per Lane	SRS			-5.4	dBm	
Peak Power, per lane	PPx			4	dBm	
Receiver Reflectance	Rfl			-12	dB	
Vertical eye closure penalty, per lane				1.9	dB	
Stressed eye J2 jitter, per Lane				0.3	UI	
Stressed eye J9 jitter, per Lane				0.47	UI	
OMA of each aggressor lane				-0.4	dBm	
Receiver jitter tolerance [OMA], per Lane				-5.4	dBm	
Rx jitter tolerance: Jitter frequency		(75, 5)			kHz, UI	
and p-p amplitude		(375, 1)			kHz, UI	

LOS De-Assert	LOSD			-11	dBm	
LOS Assert	LOSA			-14	dBm	
LOS Hysteresis		1			dB	

Notes:

1. Transmitter consists of 12 lasers operating at a maximum rate of 10.5Gb/s each.
2. Even if TDP is <0.9dB, the OMA min must exceed this value.
3. RIN is scaled by 10*log (10/4) to maintain SNR outside of transmitter.
4. Receiver consists of 12 photo-detectors operating at a maximum rate of 10.5Gb/s each.
5. Hit ratio = 5 x 10E-5
6. AC coupled with 100 Ohm differential output impedance.
7. Settable in 4 discrete steps via the I2C interface. See Figure 2 for Vout settings.

Pin Descriptions

Pin	Logic	Symbol	Name/Description	Ref.
A1		GND	Module Ground	1
A2	CML-I	Tx1+	Transmitter non-inverted data input	
A3	CML-I	Tx1-	Transmitter inverted data input	
A4		GND	Module Ground	1
A5	CML-I	Tx3+	Transmitter non-inverted data input	
A6	CML-I	Tx3-	Transmitter inverted data input	
A7		GND	Module Ground	1
A8	CML-I	Tx5+	Transmitter non-inverted data input	
A9	CML-I	Tx5-	Transmitter inverted data input	
A10		GND	Module Ground	1
A11	CML-I	Tx7+	Transmitter non-inverted data input	
A12	CML-I	Tx7-	Transmitter inverted data input	
A13		GND	Module Ground	1
A14	CML-I	Tx9+	Transmitter non-inverted data input	
A15	CML-I	Tx9-	Transmitter inverted data input	
A16		GND	Module Ground	1
A17	CML-I	Tx11+	Transmitter non-inverted data input	
A18	CML-I	Tx11-	Transmitter inverted data input	
A19		GND	Module Ground	1
A20	LVCMOS-I	SCL	2-wire Serial interface clock	2
A21	LVCMOS-I/O	SDA	2-wire Serial interface data	2
B1		GND	Module Ground	1
B2	CML-I	Tx0+	Transmitter non-inverted data input	
B3	CML-I	Tx0-	Transmitter inverted data input	
B4		GND	Module Ground	1
B5	CML-I	Tx2+	Transmitter non-inverted data input	
B6	CML-I	Tx2-	Transmitter inverted data input	
B7		GND	Module Ground	1

B8	CML-I	Tx4+	Transmitter non-inverted data input	
B9	CML-I	Tx4-	Transmitter inverted data input	
B10		GND	Module Ground	1
B11	CML-I	Tx6+	Transmitter non-inverted data input	
B12	CML-I	Tx6-	Transmitter inverted data input	
B13		GND	Module Ground	1
B14	CML-I	Tx8+	Transmitter non-inverted data input	
B15	CML-I	Tx8-	Transmitter inverted data input	
B16		GND	Module Ground	1
B17	CML-I	Tx10+	Transmitter non-inverted data input	1
B18	CML-I	Tx10-	Transmitter inverted data input	
B19		GND	Module Ground	1
B20		VCC3.3-TX	+3.3v Transmitter Power Supply	
B21		VCC12-TX	+12v Transmitter Power Supply, Unconnected	
C1		GND	Module Ground	1
C2	CML-O	RX1+	Receiver non-inverted data output	
C3	CML-O	RX1-	Receiver inverted data output	
C4		GND	Module Ground	1
C5	CML-O	RX3+	Receiver non-inverted data output	
C6	CML-O	RX3-	Receiver inverted data output	
C7		GND	Module Ground	1
C8	CML-O	RX5+	Receiver non-inverted data output	
C9	CML-O	RX5-	Receiver inverted data output	
C10		GND	Module Ground	1
C11	CML-O	RX7+	Receiver non-inverted data output	
C12	CML-O	RX7-	Receiver inverted data output	
C13		GND	Module Ground	1
C14	CML-O	RX9+	Receiver non-inverted data output	
C15	CML-O	RX9-	Receiver inverted data output	
C16		GND	Module Ground	1
C17	CML-O	RX11+	Receiver non-inverted data output	
C18	CML-O	RX11-	Receiver inverted data output	
C19		GND	Module Ground	1
C20	LVTTL-O	PRSNT_L	Module Present, pulled down to GND	
C21	LVTTL-I/O	INT_L/Reset_L	Interrupt output, Module Reset	2
D1		GND	Module Ground	1
D2	CML-O	RX0+	Receiver non-inverted data output	
D3	CML-O	RX0-	Receiver inverted data output	
D4		GND	Module Ground	1
D5	CML-O	RX2+	Receiver non-inverted data output	

D6	CML-O	RX2-	Receiver inverted data output	
D7		GND	Module Ground	1
D8	CML-O	RX4+	Receiver non-inverted data output	
D9	CML-O	RX4-	Receiver inverted data output	
D10		GND	Module Ground	1
D11	CML-O	RX6+	Receiver non-inverted data output	
D12	CML-O	RX6-	Receiver inverted data output	
D13		GND	Module Ground	1
D14	CML-O	RX8+	Receiver non-inverted data output	
D15	CML-O	RX8-	Receiver inverted data output	
D16		GND	Module Ground	1
D17	CML-O	RX10+	Receiver non-inverted data output	
D18	CML-O	RX10-	Receiver inverted data output	
D19		GND	Module Ground	1
D20		VCC3.3-RX	+3.3v Receiver Power Supply	
D21		VCC12-RX	+12v Receiver Power Supply, Unconnected	

Notes:
1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7k – 10k ohms on host board to a voltage between 3.15Vand 3.6V.

Electrical Pin-out Details

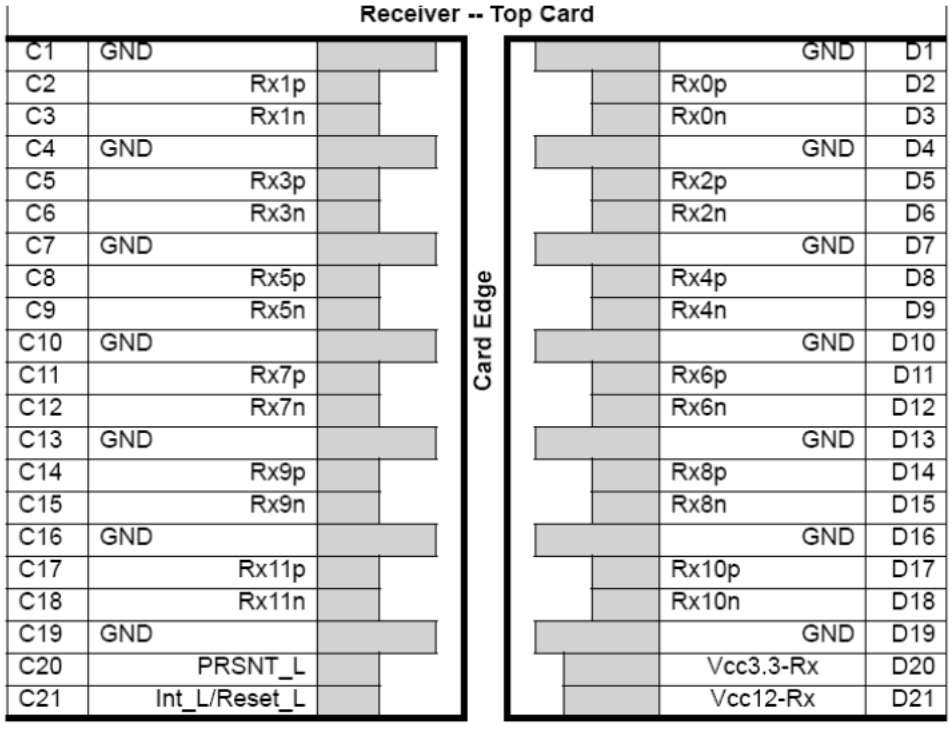

Figure2. Electrical Pin-out Details

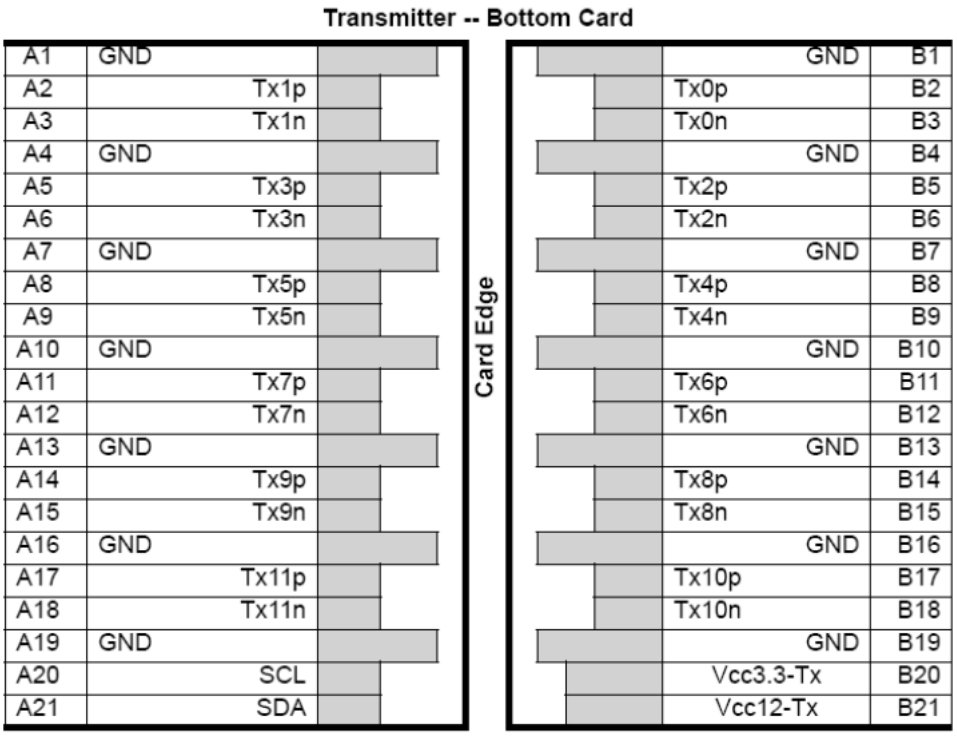

Figure2. Electrical Pin-out Details

PRSNT_L Pin：

PRSNT_L is used to indicate when the module is plugged into the host receptacle. It is pulled down to GND through 5.2 kOhm in modules requiring 12V power, and tied directly down to GND in modules requiring 3.3V power only. Sourcelight CXP Prsnt_L Pin internal directly connected to GND and just need single +3.3V Power Supply. The PRSNT_L signal is asserted “Low” when inserted and deasserted “High” when the module is physically absent from the host connector.

Int_L/Reset_L Pin：

Int_L/Reset_L is a bidirectional signal. When driven from the host, it operates logically as a Reset signal. When driven from the module, it operates logically as an Interrupt signal. In both cases, the signal is asserted low, as indicated by the ’_L’ suffix. The Int_L/Reset_L signal requires open collector outputs in both the host and module, and must be pulled up on the host board. Int_L and Reset_L indications are distinguished from each other by timing - a shorter assertion, driven by the module, indicates an interrupt, and a longer assertion of the signal, driven by the host, indicates a reset.

Int_L operation: When Int_L/Reset_L is pulled “Low” by the module for longer than the minimum interrupt pulse width (tInt_L,PW-min) and shorter than the maximum interrupt pulse width (tInt_L,PW-max) the signal signifies an interrupt. An interrupt indicates a possible module operational fault or a module status critical to the host system. The host identifies the cause of the interrupt using the 2-wire serial interface. Int_L must operate in pulse mode (vs. static mode), in order to distinguish a short interrupt signal from a longer reset signal, so the module must de-assert Int_L/Reset_L after the interrupt has been signaled.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure3.

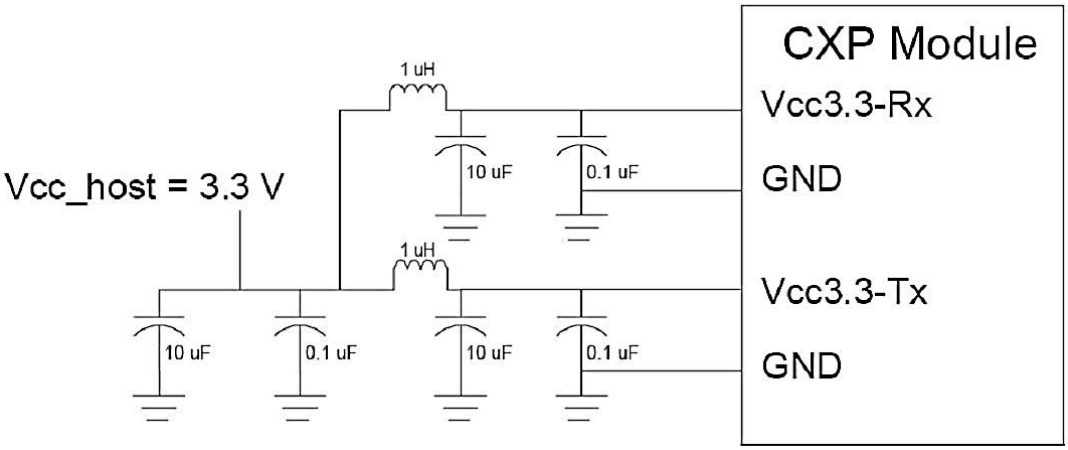

Figure3. Host Board Power Supply Filtering

Timing for Soft Control and Status Functions

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on[1], hot plug or rising edge of Reset until the module is fully functional[2]
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on[1] until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on[1] to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional[2]
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntL Deassert Time	toff_IntL	500	μs	Time from clear on read[3] operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Interrupt Pulse Max Width	tintL,PW-max	50	μs	Max Time from falling edge of int_L pin output to rising edge of int_L pin output
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Tx Fault Assert Time	ton_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set[4] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared[4] until associated IntlL operation resumes
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set [4] until module power consumption enters lower Power Level

Power_over-ride or Power-set Deassert Time	toff_Pdown	300	ms	Time from P_Down bit cleared[4] until the module is fully functional3
Interrupt Pulse Min Width	tintL,PW-min	5	μs	Min Time from falling edge of int_L pin output to rising edge of int_L pin output
Reset Pulse Min Width	Trst,PW-min	25	ms	Min Time from falling edge of Reset pin input to rising edge of Reset pin input

Note:
1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 deasserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction.

Mechanical Dimensions

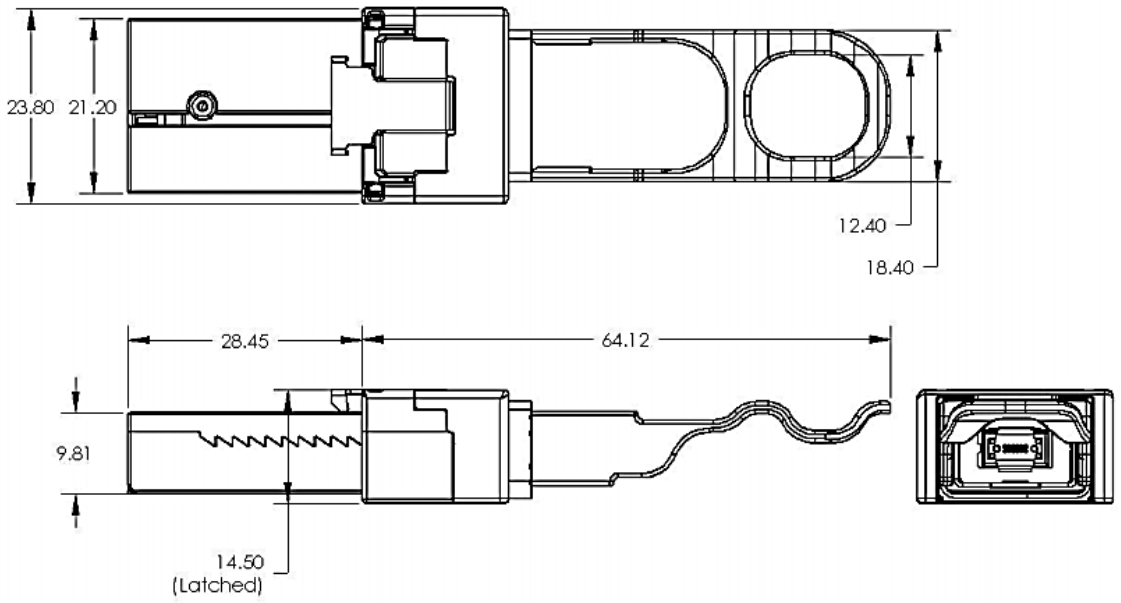

Figure5. Mechanical Specifications

References

1. 120Gbit/s Small Form-factor Hot-Pluggable CXP-interface
2. Unretimed CPPI electrical interface
3. Supplement to Infiniband Architecture Specification, Volume 2, Release 1.2.1., Annex A6: "120 Gb/s 12x Small Form-factor Pluggable (CXP) – Interface Specification for Cables, Active Cables, & Transceivers", September 2009

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